REMARKS

Applicants appreciate the examination evidenced by the final Official Action mailed October 23, 2002 and the Advisory Action mailed January 1, 2003. In response, Applicants have filed the accompanying Request for Continued Examination with this amendment which Applicants respectfully request the entry of prior to the examination of the present claims.

As discussed herein below in greater detail, Applicants have amended independent Claims 1 and 21 to further clarify the patentable subject matter recited therein. For example, independent Claim 1 has been amended to recite in part:

> forming a mask on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween, **the exposed portion of the substrate comprising a first portion where a gate electrode will be subsequently formed and a second portion where a bit line contact will be subsequently formed, the mask exposing only the first and second portions**;
>
> **implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a channel region** in only the first and second portions to adjust the threshold voltage of a transistor;
>
> forming a plurality of gate electrodes on the channel region; and
>
> implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to define separate channel regions from the channel region that are self-aligned to the plurality of gate electrodes.

Independent Claims 21 and 24 include similar recitations.

Applicants respectfully submit that the Nara reference does not disclose, for example, "**implanting ions into the exposed portion of the substrate using the mask**... **thereby forming a channel region**" and "**forming a plurality of gate electrodes on the channel region**". To the contrary, as understood by Applicants, Nara discusses first forming gate electrodes and then implanting ions to form the channel. In other words, Nara appears to discuss forming the gate electrodes before implanting the ions to form the channel. For example, Figures 1A-C of Nara illustrate

the formation of gate electrodes on the substrate 1 (in Figure 1A) and the subsequent ion implantation (in Figure 1C). Accordingly, as understood by Applicants, Nara shows ion implantation **after** the formation of gate electrodes whereas according to the amended claims, ions are implanted **before** formation of gate electrodes.

Furthermore, in discussing Figure 1B, the abstract of Nara states that a resist mask 5 (used for the channel ion implantation) exposes only a bit line contact portion of the substrate. In contrast, the amended claims recite that the exposed portion (of the substrate) comprises a first portion (of the substrate) where a gate electrode will be subsequently formed and a second portion (of the substrate) where a bit line contact will be subsequently formed. Accordingly, the amended independent claims are patentable over Nara for at least the reasons discussed above.

Applicants have also added new Claim 24 herein which recites in-part:

> forming a mask on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween;
>
> **implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a channel region in the exposed portion of the substrate** to adjust the threshold voltage of a transistor; **then**
>
> forming a plurality of gate electrodes on the channel region; and
>
> implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to define separate channel regions from the channel region that are self-aligned to the plurality of gate electrodes.

As discussed above in reference to amended independent Claims 1 and 21, Nara discusses forming implanting ions to form a channel region **before** forming a gate on the channel region. In contrast, new Claim 24 recites in part: "implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a channel region... **then** forming a plurality of gate electrodes on the channel region." According, Nara does not disclose the recitations of new Claim 24.

CONCLUSION

Applicants have amended independent Claims 1 and 21 and have added new independent Claim 24 which are patentable over Nara. Applicants respectfully request the allowance of all claims in due course. If any informal matters arise, the Examiner is encouraged to contact the undersigned by telephone at (919) 854-1400.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box RCE, Commissioner for Patents, Washington, DC 20231, on January 23, 2003.

Susan E. Freedman
Date of Signature: January 23, 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Sir:

The following is an addendum to the concurrently filed amendment in response to the final Official Action of October 23, 2002 and the Advisory Action of January 3, 2003 in the above referenced application. This addendum includes a marked-up version of the changes made to the claims by the present amendment.

In the Claims:

Claims 1 and 21 have been amended as follows:

1. (Twice Amended) A method of forming a channel region between isolation regions of an integrated circuit substrate, the method comprising:

forming a mask on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween, the exposed portion of the substrate comprising a first portion where a gate electrode will be subsequently formed and a second portion where a bit line contact will be subsequently formed, the mask exposing only the first and second portions;

implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a channel region in only the first and second portions [the exposed portion of the substrate] to adjust the threshold voltage of a transistor;

forming a plurality of gate electrodes on the channel region; and

implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to define separate channel regions from the channel region that are self-aligned to the plurality of gate electrodes.

21. (Amended) A method of forming a channel region between isolation regions of an integrated circuit substrate, the method comprising:

forming a mask on first and second adjacent isolation regions in an integrated circuit substrate and extending onto an active area between the first and second

adjacent isolation regions to define first and second shielded portions of the substrate adjacent to the first and second isolation regions and an exposed portion of the substrate therebetween, the exposed portion of the substrate comprising a first portion where a gate electrode will be subsequently formed and a second portion where a bit line contact will be subsequently formed, the mask exposing only the first and second portions;

implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a single channel region in only the first and second portions [the exposed portion of the substrate] to adjust the threshold voltage of a transistor;

forming a plurality of gate electrodes on the single channel region; and

implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to form first and second spaced apart channel regions from the single channel region.

The following new Claim 24 has been added:

24. (New) A method of forming a channel region between isolation regions of an integrated circuit substrate, the method comprising:

forming a mask on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween;

implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a channel region in the exposed portion of the substrate to adjust the threshold voltage of a transistor; then

forming a plurality of gate electrodes on the channel region; and

implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to define separate channel regions from the channel region that are self-aligned to the plurality of gate electrodes.

END